IN THE CLAIMS

Kindly amend claims 8, 17, 18, and cancel claims 16, 20, all without prejudice so that the claims appear as follows.

1. (Withdrawn) A method of forming a semiconductor structure, comprising:

providing a substrate having a first semiconductor layer positioned on a first insulator layer, a second insulator layer positioned on said first semiconductor layer, and a second semiconductor layer positioned on said second insulator layer;

forming a first fin and a second fin in said second semiconductor layer;

masking said first fin; and

forming a third fin in said first semiconductor layer, wherein said second fin is stacked on said third fin.

2. (Withdrawn) The method of claim 1, wherein the step of forming said first fin and said second fin comprises:

depositing a hardmask layer on said second semiconductor layer;

patterning said hardmask layer; and

etching said second semiconductor layer to form said first fin and said second fin.

3. (Withdrawn) The method of claim 2, wherein said etching of said second semiconductor layer stops when said second insulator layer is reached.

4. (Withdrawn) The method of claim 1, wherein the step of forming said third fin comprises:

depositing and developing a photoresist over said first fin; and

etching said second insulator layer and said first semiconductor layer to form said third fin.

5. (Withdrawn) The method of claim 4, wherein said etching of said first semiconductor layer stops when said first insulator layer is reached.

6. (Withdrawn) The method of claim 1, further comprising the steps of:

implanting a dopant into each of said fins;

forming a gate insulator layer on opposing sidewalls of each of said fins;

forming a gate conductor layer on said gate insulator layer;

patterning said gate conductor layer and said gate insulator layer; wherein said patterning forms gate stacks;

implanting a source region in a first exposed portion of each of said fins;

implanting a drain region in a second exposed portion of each of said fins, wherein said source and drain regions are separated by a channel region; and

forming contacts to said source region, said drain region and said gate conductor layer.

7. (Withdrawn) The method of claim 6, wherein said contacts are formed by:

depositing a dielectric layer;

planarizing said dielectric layer;

etching openings in said planarized dielectric layer; and

filing said openings with a conducting material, wherein said filled openings form said contacts.

8. (Currently Amended) A semiconductor structure, comprising:

a semiconductor substrate having a first semiconductor layer positioned on a first insulator layer, a second insulator layer positioned on said first semiconductor layer, and a second semiconductor layer positioned on said second insulator layer;

a first and second fin formed in said second semiconductor layer; and

a third fin formed in said first semiconductor layer, wherein said second fin is stacked on said third fin,

and wherein said first semiconductor layer has a surface oriented on a first crystal plane and said second semiconductor layer has a surface oriented on a second crystal plane, said first crystal plane being oriented differently than said second crystal plane, and wherein said surface oriented on said first crystal plane is substantially parallel to said surface oriented on said second crystal plane.

9. (Original) The semiconductor structure of claim 8, wherein said stacked fins form a first finFET and said first fin forms a second finFET.

10. (Original) The semiconductor structure of claim 9, wherein said first finFET is a p-channel finFET and said second finFET is a n-channel finFET.

11. (Original) The semiconductor structure of claim 8, wherein said second semiconductor layer is bonded to said second insulator layer.

12. (Original) The semiconductor structure of claim 8, wherein a height of said third fin corresponds to a thickness of said first semiconductor layer.

13. (Original) The semiconductor structure of claim 12, wherein said first semiconductor layer thickness ranges approximately from 40 nm to 70 nm.

14. (Original) The semiconductor structure of claim 8, wherein a height of said first fin and said second fin correspond to a thickness of said second semiconductor layer.

15. (Original) The semiconductor structure of claim 14, wherein said second semiconductor layer thickness ranges approximately from 40 nm to 70 nm.

16. (Cancelled) The semiconductor structure of claim 8, wherein said first semiconductor layer has a surface oriented on a first crystal plane and said second semiconductor layer has a surface oriented on a second crystal plane.

17. (Currently Amended) The semiconductor structure of claim 8, ~~16,~~ wherein a first mobility is associated with said first crystal plane and a second mobility is associated with said second crystal plane, wherein said first mobility is different from said second mobility.

18. (Currently Amended) The semiconductor structure of claim 8, ~~16,~~ wherein sidewalls of said first and second fins are orientated on a {100} crystal plane and sidewalls of said third fin are oriented on a {110} crystal plane.

19. (Original) The semiconductor structure of claim 8, further comprising:

a dopant implanted into each of said fins;

a gate insulator layer formed on opposing sidewalls of each of said fins;

a gate conductor layer formed on said gate insulator layer, wherein said gate conductor layer and said gate insulator layer form gate stacks;

a source region implanted in a first exposed portion of each of said fins; and

a drain region implanted in a second exposed portion of each of said fins, wherein said source and drain regions are separated by a channel region.

20. (Cancelled) A circuit, comprising:

a first semiconductor layer positioned on a first insulator layer;

a second insulator layer positioned on said first semiconductor layer;

a second semiconductor layer positioned on said second insulator layer;

a first and second fin formed in said second semiconductor layer; and

a third fin formed in said first semiconductor layer, wherein said second fin is stacked on said third fin.